DELKIN DEVICES®

D330 Series

Industrial Temperature Secure Digital

Engineering Specification

Document Number: 401-0506-00
Revision: A

Overview

- **Capacity**
  - 128MB up to 32GB
- **Bus Speed Mode**
  - 4GB and above: UHS I
  - 2GB and below: non UHSI
- **Flash Interface**
  - Flash Type: SLC
- **Power Consumption**[Note1]
  - Power Up Current < 250uA
  - Standby Current < 1mA
  - Read Current < 400mA
  - Write Current < 400mA
- **Performance**
  - Read: Up to 95 MB/s
  - Write: Up to 90 MB/s
- **CPRM (Content Protection for Recordable Media)**
- **MTBF**
  - More than 3,000,000 hours
- **Advanced Flash Management**
  - Static and Dynamic Wear Leveling
  - Bad Block Management
  - SMART Function
  - Auto-Read Refresh
  - Embedded Mode
- **Storage Temperature Range**
  - -40°C ~ 85°C
- **Operation Temperature Range**
  - -40°C ~ 85°C
- **RoHS compliant**
- **EMI compliant**

Notes:

1. Varies by capacity, please see Section “5.1 Power Consumption” for details.

Performance and Power Consumption

Capacity	Performance		Power Consumption (Maximum)		
	TestMetrixTest @500MB		Read (mA)	Write (mA)	Standby (uA)
	Read (MB/s)	Write (MB/s)			
128MB	20	4	400	400	1
256MB	20	9	400	400	1
512MB	20	15	400	400	1
1GB	20	20	400	400	1
2GB	20	20	400	400	1
4GB	30	25	400	400	1
8GB	65	50	400	400	1
16GB	65	55	400	400	1
32GB	65	65	400	400	1

NOTE:

For more details on Power Consumption, please refer to Section 5.1.

Power Consumption figures shown are maximum values and may vary with usage model, SDR configuration or host platform.

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1. INTRODUCTION

1.1. General Description

Delkin's SLC D330 Series Secure Digital (SD) card is fully compliant with the specification released by the SD Card Association and offers a full industrial temperature range. The Command List supports [Part 1 Physical Layer Specification Version 3.01 Final] definitions and Card Capacity of Non-secure Area, Secure Area Supports [Part 3 Security Specification Ver 3.00 Final] Specifications.

The D330 card utilizes the standard 9-pin interface, designed to operate at a maximum operating frequency of 100MHz. It can alternate between SD mode and SPI mode communication protocols. SD also has the benefits of lower power consumption and high capacity, up to 128GB, in a small package.

Delkin's D330 Secure Digital card is an extremely popular choice today based on its high performance, good reliability and wide compatibility. It is ideal for OEM applications in semi-industrial, medical, handheld, and other markets requiring a controlled, yet cost-effective solution.

1.2. Flash Management

1.2.1. Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, Delkin's D330 series SD controller applies the BCH ECC Algorithm, which can detect and correct errors that occur during the Read process, ensure data has been read correctly, as well as protect data from corruption.

1.2.2. Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas are updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling techniques are applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media. Delkin's D330 series SD controller utilizes an advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND Flash is greatly improved.

1.2.3. Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as "Initial Bad Blocks". Bad blocks that are developed during the lifespan of the flash are named "Later Bad Blocks". Delkin's D330 series SD controller implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that develop with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

1.2.4. Smart Function

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is a special function that allows a memory device to automatically monitor its health. Delkin provides a dashboard to observe Utility+ SD and microSD cards. **Note that this tool can only support Delkin Utility / Utility+ or Industrial SD and microSD cards which are SMART-enabled and contain specific controllers.** This dashboard will display the controller version, flash type, firmware version, endurance life ratio, good block ratio, and so forth. In addition, a warning message will appear under the following 3 conditions:

(1) When the life ratio remained is less than **10%**,

(2) When the amount of abnormal power on is more than **3,500** cycles, and

(3) When there are less than **5** usable blocks for replacing bad blocks.

1.2.5. Auto-Read Refresh

Auto-Read Refresh is especially applied on devices that mostly read data but rarely write data, GPS systems, for example. When blocks are continuously read, then the device cannot activate wear leveling since it is only applied while writing data. Thus, errors can accumulate and become uncorrectable. Therefore, to avoid the accumulation of errors that exceed the quantity correctable by the controller's ECC, which would result in bad blocks, Delkin's controller firmware will automatically refresh the bit errors when the error number in one block approaches the threshold, ex., 24 bits.

1.2.6. Data Clone System (DCS)

DCS is a function which minimizes the chance of data loss in the event of sudden power interruption. When power loss occurs during writing, there will always be a chance for data become corrupted. To counter this, Delkin's SD controller firmware will write an extra copy of the data to a buffer block. In the event of a sudden power loss, during the next power up, ECC will be checked on the original target block. If ECC was discovered, the firmware will copy the data from the buffer block and replace the corrupted data in the original target block. This will greatly reduce the chance of the corrupted data.

1.2.7. Embedded Mode

Embedded mode is a function specially designed for Linux or customized OS use. Often under non-Windows OS, the default FAT system will not be used. In this case, the wear leveling mechanism of the SD cards will be affected, or even disabled in some cases. Embedded mode ensures that under any circumstances, the wear leveling mechanism will be activated, to keep the usage of blocks even throughout the card's life cycle.

2. PRODUCT SPECIFICATION OVERVIEW

- **Capacity**

  128MB up to 32GB

- **Operation Temp. Range**
  - -40 ~ +85°C
- **Storage Temp. Range**
  - -40 ~ +85°C
- **Support SD system specification version 3.0**
- **Card capacity of non-secure area and secure area support [Part 3 Security Specification Ver3.0 Final] Specifications**
- **Support SD SPI mode**
- **Designed for read-only and read/write cards**
- **Bus Speed Mode (use 4 parallel data lines)**
  - UHS-I mode
    - SDR104: 1.8V signaling, frequency up to 208MHz, up to 104MB/sec

  Note: Timing in 1.8V signaling is different from that of 3.3V signaling.
- **The command list supports [Part 1 Physical Layer Specification Ver3.01 Final] definitions**
- **Copyright Protection Mechanism**
  - Compliant with the highest security of SDMI standard
- **Supports CPRM (Content Protection for Recordable Media) of SD Card**
- **Card removal during read operation will never harm the content**
- **Password Protection of cards (optional)**
- **Write Protect feature using mechanical switch**
- **Built-in write protection features (permanent and temporary)**
- **+4KV/-4KV ESD protection in contact pads**
- **Operation voltage range: 2.7 ~ 3.6V**

2.1. Performance

Capacity	Mode	Sequential	
		Read (MB/s)	Write (MB/s)
128MB	non UHS	20	4
256MB	non UHS	20	9
512MB	non UHS	20	15
1GB	non UHS	20	20
2GB	non UHS	20	20
4GB	UHS-I	30	25
8GB	UHS-I	65	50
16GB	UHS-I	65	55
32GB	UHS-I	65	65

NOTES:

1. Benchmark performance measured with TestMetrix Test (@500MB).

2.2. Part Numbers

D330 SD

Capacity	Part Number
128MB	SE12TLKFX-1D000-3
256MB	SE25TLMFX-1D000-3
512MB	SE51TLNFX-1D000-3
1GB	SE0GTLNFX-1D000-3
2GB	SE02TLNFX-1D000-3
4GB	SE04TLNFX-1B000-3
8GB	SE08TRZFX-1B000-3
16GB	SE16TRZFX-1B000-3
32GB	SE32TRZFX-1B000-3

3. ENVIRONMENTAL SPECIFICATIONS

3.1. Environmental Conditions

3.1.1. Temperature and Humidity

- Storage Temperature Range
  - -40°C ~ +85°C
- Operation Temperature Range
  - -40°C ~ +85°C
- Humidity
  - 95% RH under 55°C

3.1.2. Shock & Vibration

- Shock Specification
  - 1500G, 0.5ms duration
- Vibration Specification
  - 20Hz ~80Hz/1.52mm displacement, 80Hz~2000Hz / 20G Acceleration, 3 axes

3.1.3. Durability

- Mating Cycles
  - 10,000 mating cycles

3.1.4. Electrostatic Discharge (ESD)

- Contact
  - ± 4KV
- Air
  - ± 8KV

3.1.5. EMI Compliance

- FCC: CISPR22
- CE: EN55022
- BSMI 13438

3.2. MTBF

MTBF, an acronym for Mean Time Between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The measure is typically in units of hours. The higher the MTBF value, the higher the reliability of the device. The predicted result of Delkin's D330 Series SD is more than 3,000,000 hours..

4. SD CARD COMPARISON

Table 4-1 Comparing SD3.0 Standard, SD3.0 SDHC, SDXC

	SD3.0 Standard (Backward compatible to 2.0 host)	SD3.0 SDHC (Backward compatible to 2.0 host)	SD3.0 SDXC
Addressing Mode	Byte (1 byte unit)	Block (512 byte unit)	Block (512 byte unit)
HCS/CCS bits of ACMD41	Supported	Supported	Supported
CMD8 (SEND_IF_COND)	Supported	Supported	Supported
CMD16 (SET_BLOCKLEN)	Supported	Supported (Only CMD42)	Supported (Only CMD42)
Partial Read	Supported	Not Supported	Not Supported
Lock/Unlock Function	Mandatory	Mandatory	Mandatory
Write Protect Groups	Optional	Not Supported	Not Supported
Supply Voltage 2.0v – 2.7v (for initialization)	Not Supported	Not Supported	Not Supported
Total Bus Capacitance for each signal line	40pF	40pF	40pF
CSD Version (CSD_STRUCTURE Value)	1.0 (0x0)	2.0 (0x1)	2.0 (0x1)
Speed Class	Optional	Mandatory (Class 2 / 4 / 6 / 10)	Mandatory (Class 2 / 4 / 6 / 10)

5. ELECTRICAL SPECIFICATIONS

5.1. Power Consumption

The table below is the power consumption of Delkin SD by capacity.

Table 5-1 Power Consumption by Capacity (Maximum)

Capacity	Read (mA)	Write (mA)	Standby (uA)
128MB	400	400	1
256MB	400	400	1
512MB	400	400	1
1GB	400	400	1
2GB	400	400	1
4GB	400	400	1
8GB	400	400	1
16GB	400	400	1
32GB	400	400	1

NOTE:

1. Power Consumption shown is maximum and will vary by usage model, SDR configuration, or platform.

5.2. DC Characteristic

5.2.1. Bus Operation Conditions for 3.3V Signaling

Table 5-2 Threshold Level for High Voltage Range

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	VDD	2.7	3.6	V	
Output High Voltage	VOH	0.75*VDD		V	IOH=-2mA VDD Min
Output Low Voltage	VOL		0.125*VDD	V	IOL=2mA VDD Min
Input High Voltage	VIH	0.625*VDD	VDD+0.3	V	
Input Low Voltage	VIL	VSS-0.3	0.25*VDD	V	
Power Up Time			250	Ms	From 0V to VDD min

Table 5-3 Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max.	Unit	Remarks
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

Table 5-4 Threshold Level for 1.8V Signaling

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	VDD	2.7	3.6	V	
Regulator Voltage	VDDIO	1.7	1.95	V	Generated by VDD
Output High Voltage	VOH	1.4	-	V	IOH=-2mA
Output Low Voltage	VOL	-	0.45	V	IOL=2mA
Input High Voltage	VIH	1.27	2.00	V	
Input Low Voltage	VIL	Vss-0.3	0.58	V	

Table 5-5 Input Leakage Current for 1.8V Signaling

Parameter	Symbol	Min	Max.	Unit	Remarks
Input Leakage Current		-2	2	uA	DAT3 pull-up is disconnected.

5.2.2. Bus Signal Line Load

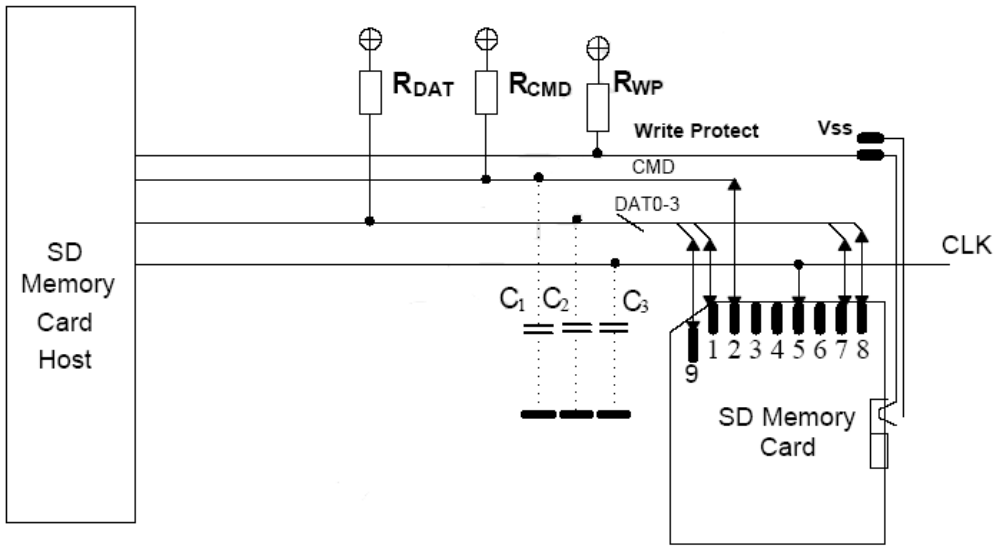


Figure 5-1 Bus Circuitry Diagram

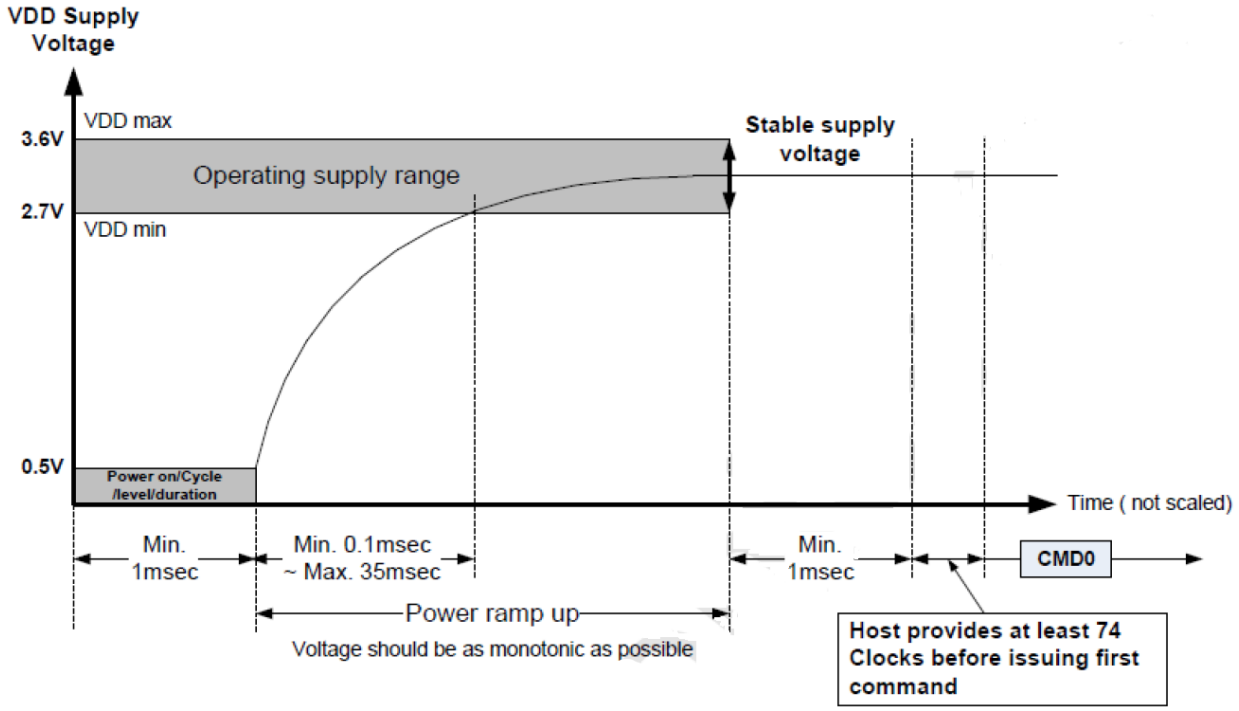
Bus Operation Conditions – Signal Line's Load

Total Bus Capacitance = CHOST + CBUS + N CCARD

Parameter	symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card CHOST+CBUS shall not exceed 30 pF
Card Capacitance for each signal pin	CCARD		10	pF	
Maximum signal line inductance			16	nH	
Pull-up resistance inside card (pin1)	RDAT3	10	90	kΩ	May be used for card detection
Capacity Connected to Power Line	CC		5	uF	To prevent inrush current

5.2.3. Power Up Time

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.



Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable SD Card hard reset.

(1) Voltage level shall be below 0.5V.
(2) Duration shall be at least 1ms.

Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD (min.) and VDD (max.) and host can supply SDCLK.

Followings are recommendations of Power ramp up:

(1) Voltage of power ramp up should be monotonic as much as possible.
(2) The minimum ramp up time should be 0.1ms.
(3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.

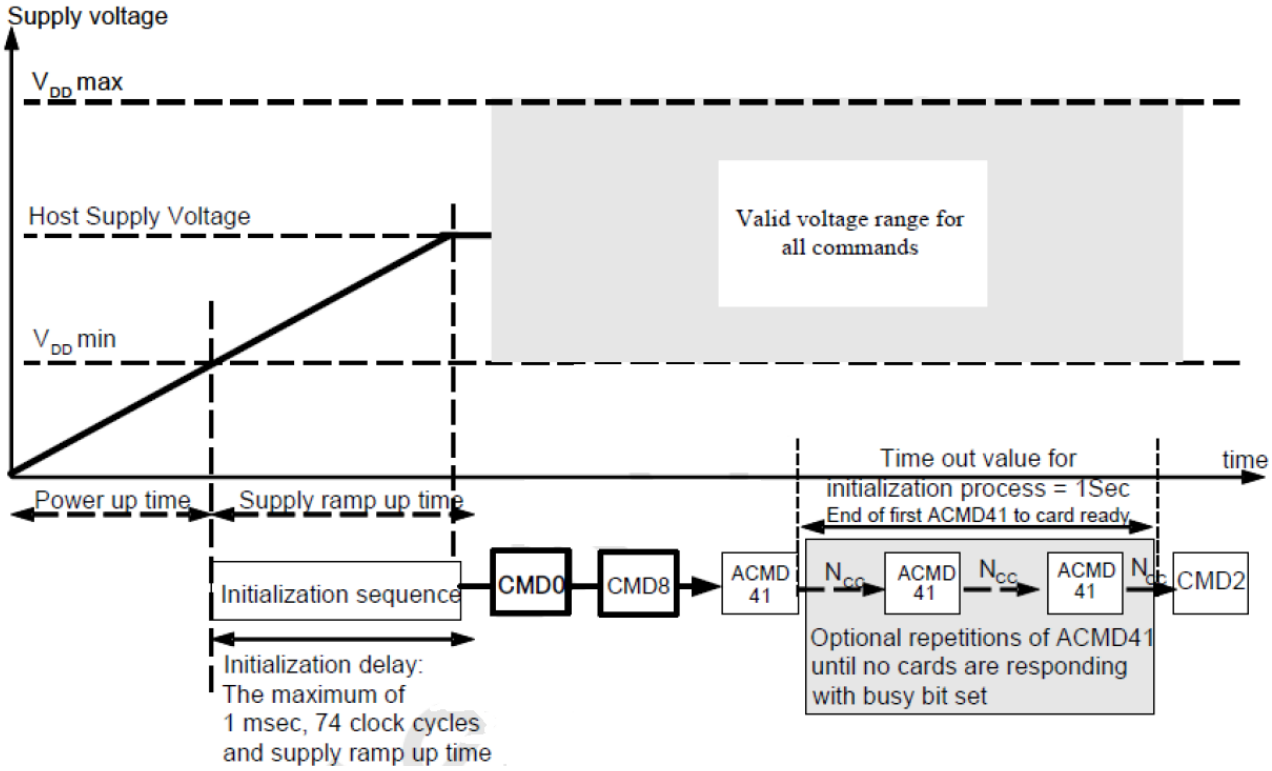
Power Down and Power Cycle

(1) When the host shuts down the power, the card VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.
(2) If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing

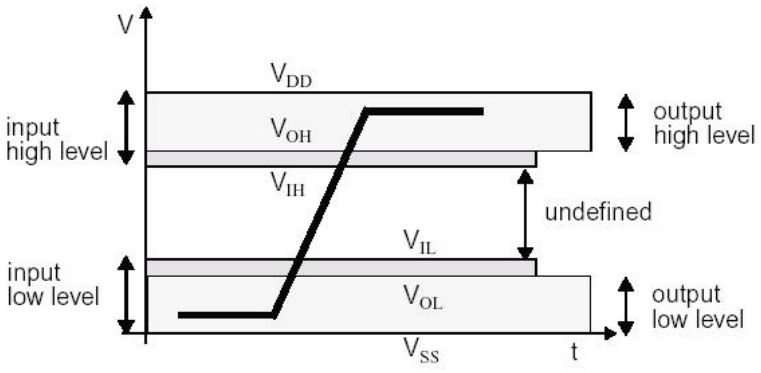
cards that are already in *Inactive State.* To create a power cycle the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

5.2.4. Power Up Time of Card

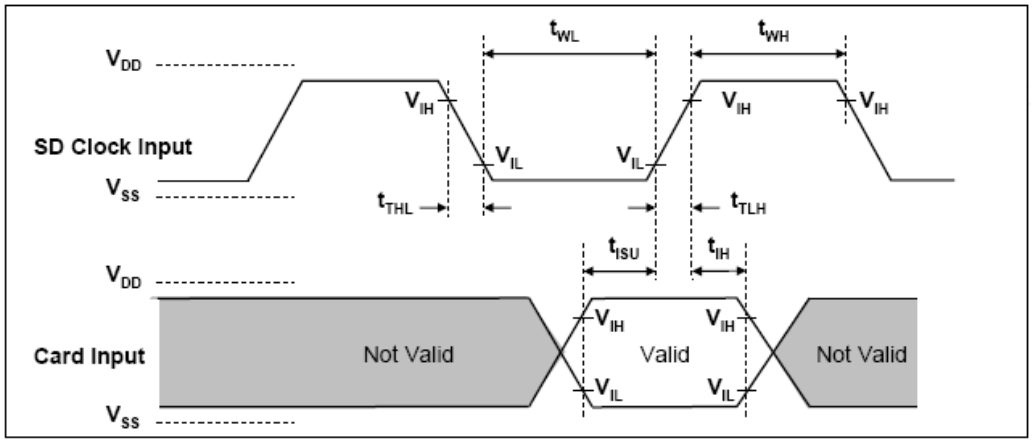
A device shall be ready to accept the first command within 1ms from detecting VDD min.Device may use up to 74 clocks for preparation before receiving the first command.



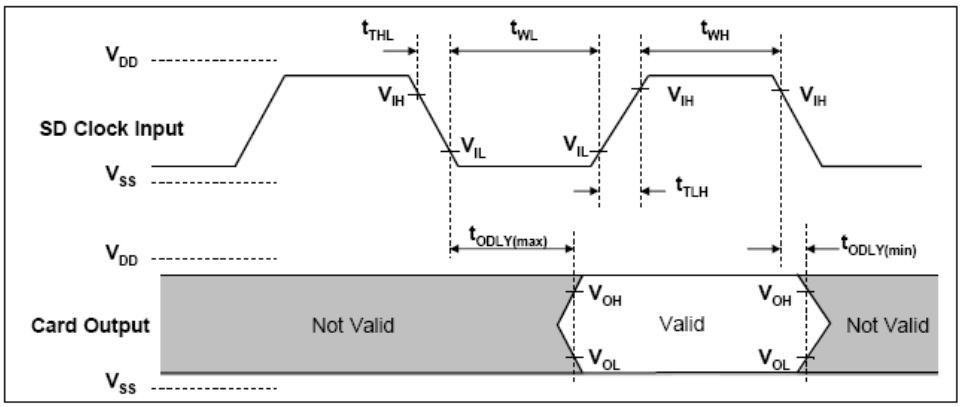
5.3. AC Characteristic



5.3.1. SD Interface Timing (Default)



Card Input Timing (Default Speed Card)



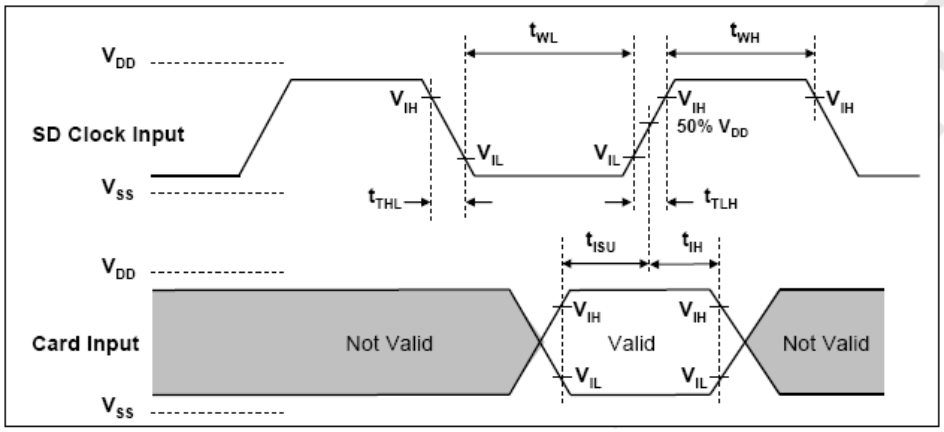
Card Output Timing (Default Speed Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{card}≤□10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	0(1)/100	400	kHz	C_{card}≤□10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{card}≤□10 pF (1 card)
Clock high time	t_{WH}	10		ns	C_{card}≤□10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{card}≤□10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{card}≤□10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{card}≤□10 pF (1 card)
Input hold time	t_{IH}	5		ns	C_{card}≤□10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data	t_{ODLY}	0	14	ns	C_L≤40 pF

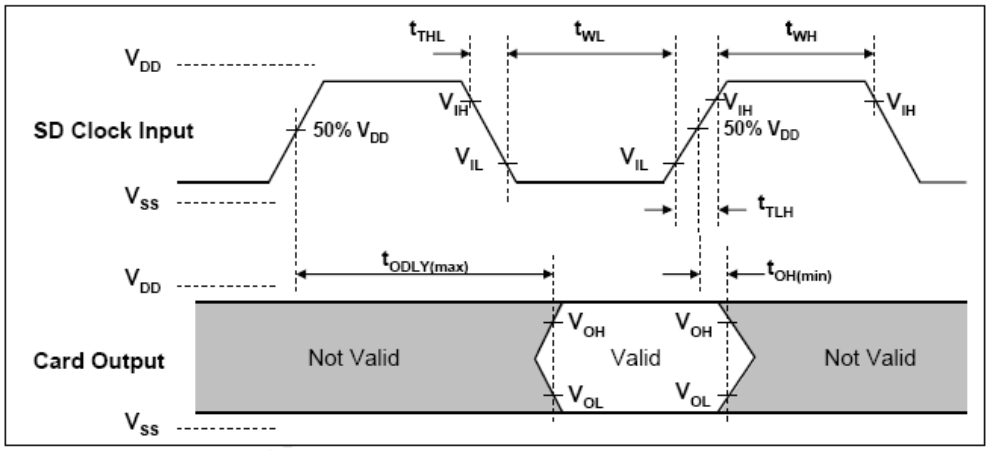
Transfer Mode					(1 card)
Output Delay time during Identification Mode	tODLY	0	50	ns	C_L≤40 pF (1 card)

(1) 0Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required.

5.3.2. SD Interface Timing (High-Speed Mode)



Card Input Timing (High Speed Card)



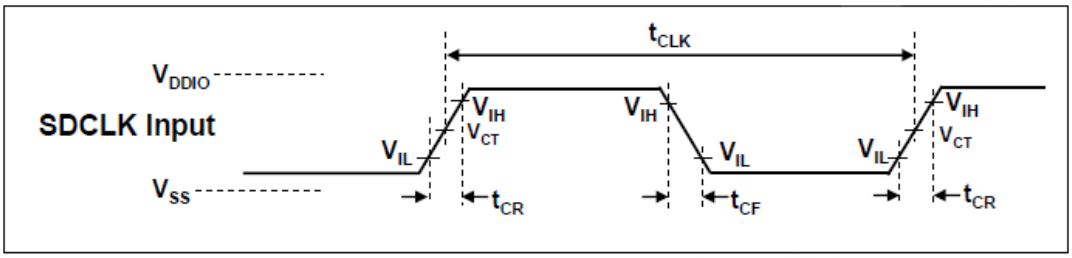
Card Output Timing (High Speed Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{card} ≤ 10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{card} ≤ 10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{card} ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{card} ≤ 10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{card} ≤ 10 pF (1 card)
Input hold time	t_{IH}	2		ns	C_{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	C_L ≤ 40 pF (1 card)
Output Hold time	T_{OH}	2.5		ns	C_L ≤ 15 pF (1 card)
Total System capacitance of each line[1]	C_L		40	pF	CL ≤ 15 pF (1 card)

(1) In order to satisfy severe timing, the host shall drive only one card.

5.3.3. SD Interface Timing SD Interface Timing (SDR12, SDR25 , SDR 50 and SDR 104 Modes)

Input

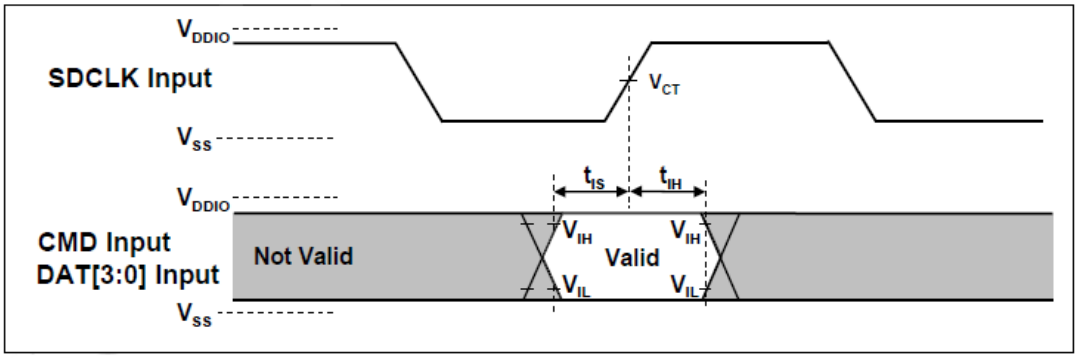


Clock Signal Timing

Table 5-6 Clock Signal Timing

Symbol	Min	Max	Unit	Remark
tCLK	4.80	-	ns	208MHz (Max.), Between rising edge, VCT= 0.975V
tCR, tCF	-	0.2* tCLK	ns	tCR, tCF < 2.00ns (max.) at 100MHz, CCARD=10pF
Clock Duty	30	70	%	

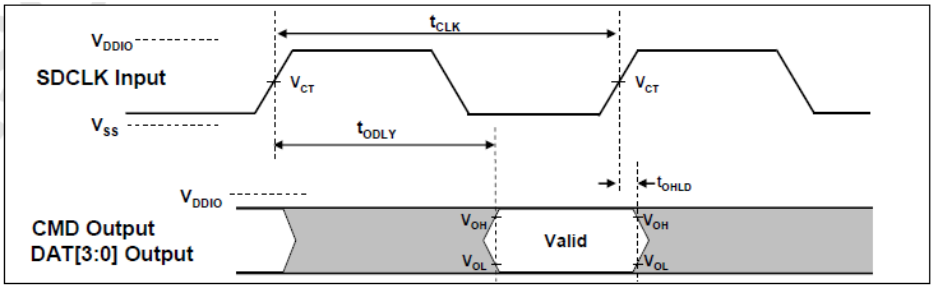
SDR50 and SDR104 Input Timing



Card Input Timing

Symbol	Min	Max	Unit	SDR104 Mode
tIs	1.40	-	ns	CCARD =10pF, VCT= 0.975V
tIH	0.80	-	ns	CCARD =5pF, VCT= 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 Mode**
tIs	3.00	-	ns	CCARD =10pF, VCT= 0.975V
tIH	0.80	-	ns	CCARD =5pF, VCT= 0.975V

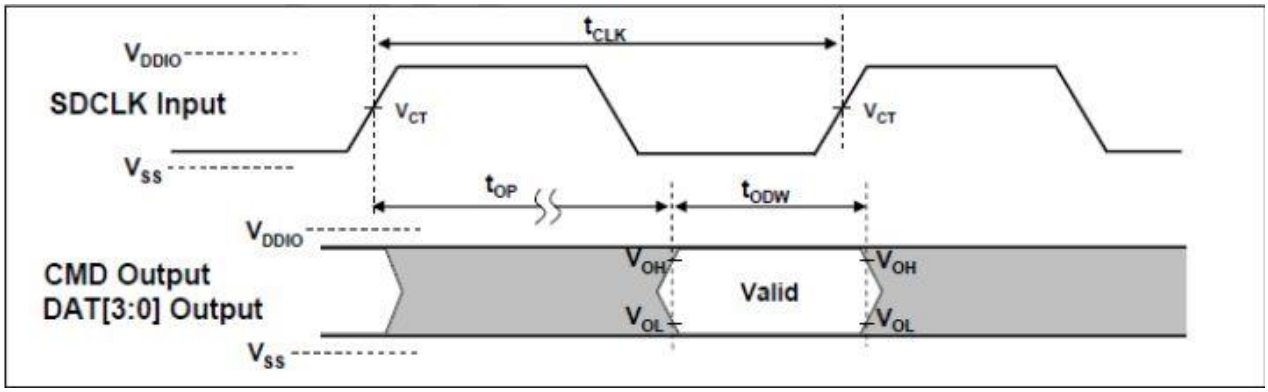
Output(SDR12, SDR25, SDR50)



Output Timing of Fixed Data Window

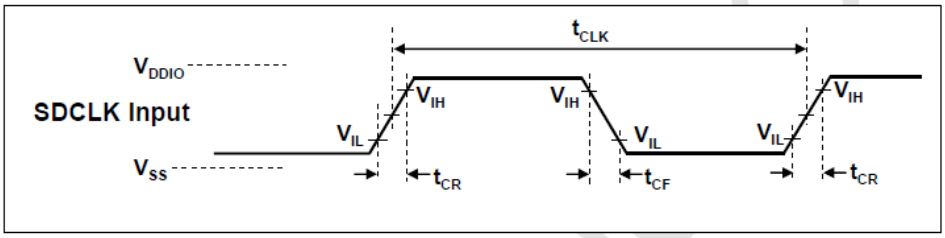
Table 5-7 Output Timing of Fixed Data Window (SDR12, SDR25, SDR50 Modes)

Symbol	Min	Max	Unit	Remark
tODLY	-	7.5	ns	tCLK>=10.0ns, CL=30pF, using driver Type B, for SDR50
tODLY	-	14	ns	tCLK>=20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12,
TOH	1.5	-	ns	Hold time at the tODLY (min.), CL=15pF



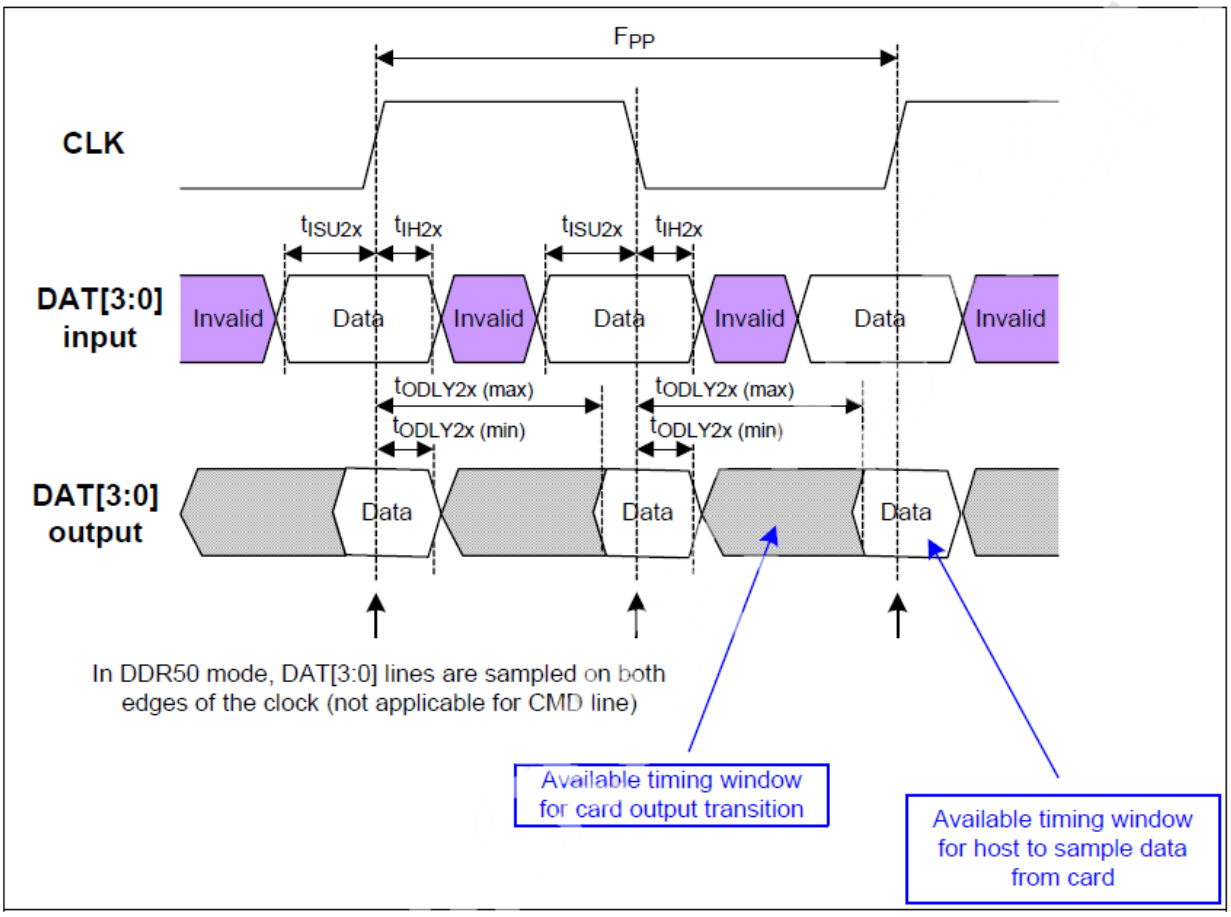
Symbol	Min	Max	Unit	Remark
tOP	0	2	UI	Card Output Phase
Δ tOP	-350	+1550	ps	Delay variable due to temperature change after tuning
tODW	0.60	-	UI	tODW = 2.88ns at 208MHz

5.3.4. SD Interface Timing (DDR50 Mode)



Clock Signal Timing

Symbol	Min	Max	Unit	Remark
tCLK	20	-	ns	50MHz (Max.), Between rising edge
tCR, tCF	-	0.2* tCLK	ns	tCR, tCF < 4.00ns (max.) at 50MHz, CCARD=10pF
Clock Duty	45	55	%	



Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

Table 5-8 Bus Timings – Parameters Values (DDR50 Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	6	-	ns	C_{card}≤□10 pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{card}≤□10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	C_L≤30 pF (1 card)
Output Hold time	T_{OH}	1.5	-	ns	C_L≥15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	C_{card}≤□10 pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{card}≤□10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	C_L≤25 pF (1 card)
Output Hold time	T_{OH2x}	1.5	-	ns	C_L≥15 pF (1 card)

6. INTERFACE

6.1. Pad Assignment and Descriptions

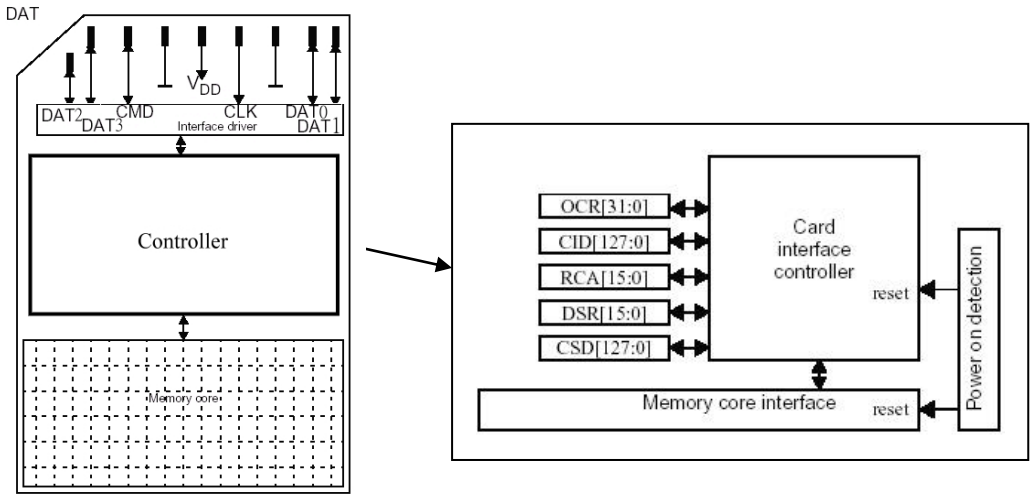


Table 6-1 SD Memory Card Pad Assignment

pin	SD Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type	Description
1	CD/DAT3 [2]	I/O/PP [3]	Card Detect/ Data Line[bit3]	CS	I [3]	Chip Select (net true)
2	CMD	PP	Command/Response	DI	I	Data In
3	V_{SS1}	S	Supply voltage ground	VSS	S	Supply voltage ground
4	V_{DD}	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS2}	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line[bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line[bit1]	RSV		
9	DAT2	I/O/PP	Data Line[bit2]	RSV		

(1) S: power supply, I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers.

(2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode as well while they are not used. It is defined so in order to keep compatibility to MultiMedia Cards.

(3) At power up, this line has a 50KOhm pull up enabled in the card. This resistor serves two functions: Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode, it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer with SET_CLR_CARD_DETECT (ACMD42) command.

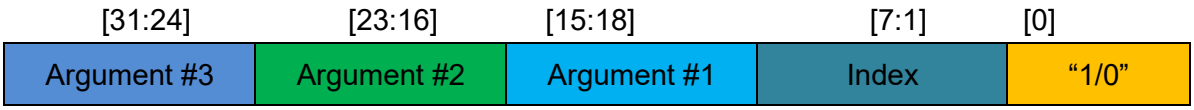
Name	Width	Description
CID	128bit	Card identification number; card individual number for identification. **Mandatory**
RCA1	16bit	Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization. **Mandatory**
DSR	16bit	Driver Stage Register; to configure the card's output drivers. **Optional**
CSD	128bit	Card Specific Data; information about the card operation conditions. **Mandatory**
SCR	64bit	SD Configuration Register; information about the SD Memory Card's Special Features capabilities **Mandatory**
OCR	32bit	Operation conditions register. **Mandatory.**
SSR	512bit	SD Status; information about the card proprietary features **Mandatory**
OCR	32bit	Card Status; information about the card status **Mandatory**

(1) RCA register is not used (or available) in SPI mode.

7. SMART

7.1. Direct Host Access to SMART Data via SD General Command (CMD56)

CMD 56 is structured as a 32-bit argument. The implementation of the general purpose functions will arrange the CMD56 argument into the following format:



Bit [0] Indicates Read Mode when bit is set to [1] or Write Mode when bit is cleared [0]. Depending on the function, either Read Mode or Write Mode can be used.

Bit [7:1] Indicates the index of the function to be executed:

- Read Mode
  - Index = 0x10 Get SMART Command Information
- Write Mode
  - Index = 0x08 Pre-Load SMART Command Information

Bit [15:8] Function argument #1 (1-byte)

Bit [23:16] Function argument #2 (1-byte)

Bit [31:24] Function argument #3 (1-byte)

7.1.1. Process for Retrieving SMART Data

STEP 1:

Write Mode – [0x08] Pre-Load SMART Command Information

Sequence	Command	Argument	Expected Data
Pre-Load SMART Command Information	CMD56	[0] "0" (Write Mode) [1:7] "0001 000" (Index = 0x08) [8:511] All '0' Reserved)	No Expected Data

STEP 2:

Read Mode – [0x10] Get SMART Command Information

Sequence	Command	Argument	Expected Data
Get SMART Command Information	CMD56	[0] "1" (Read Mode) [1:7] "0010 000" (Index = 0x10) [8:511] All '0' Reserved)	1 sector (512 bytes) of response data Byte [0-8] Flash ID Byte [9-10] IC Version Byte [11-12] FW Version Byte [13] Reserved Byte [14] CE Number Byte [15] Reserved Byte [16-17] Maximum Bad Block Replacement Byte [18] Reserved Byte [32-63] Bad Block Count per CE Byte [64-65] Good Block Rate (%) Byte [66-79] Reserved Byte [80-83] Total Erase Count Byte [84-95] Reserved Byte [96-97] Calculated Remaining Life (%) Byte [98-99] Average Erase Count Byte [100-101] Minimum Erase Count Byte [102-103] Maximum Erase Count Byte [104-111] Reserved Byte [112-115] Power Cycle Count Byte [116-127] Reserved Byte [128-129] Abnormal Power Down Count Byte [130-159] Reserved Byte [160-161] Total Refresh Count Byte [176-183] Product "Marker" Byte [184-511] Reserved

Note: Both steps are required to retrieve SMART data - Pre-Load SMART Command followed by Get SMART Command, and must be in accordance with the SD Association standard flowchart for CMD56 (below.)

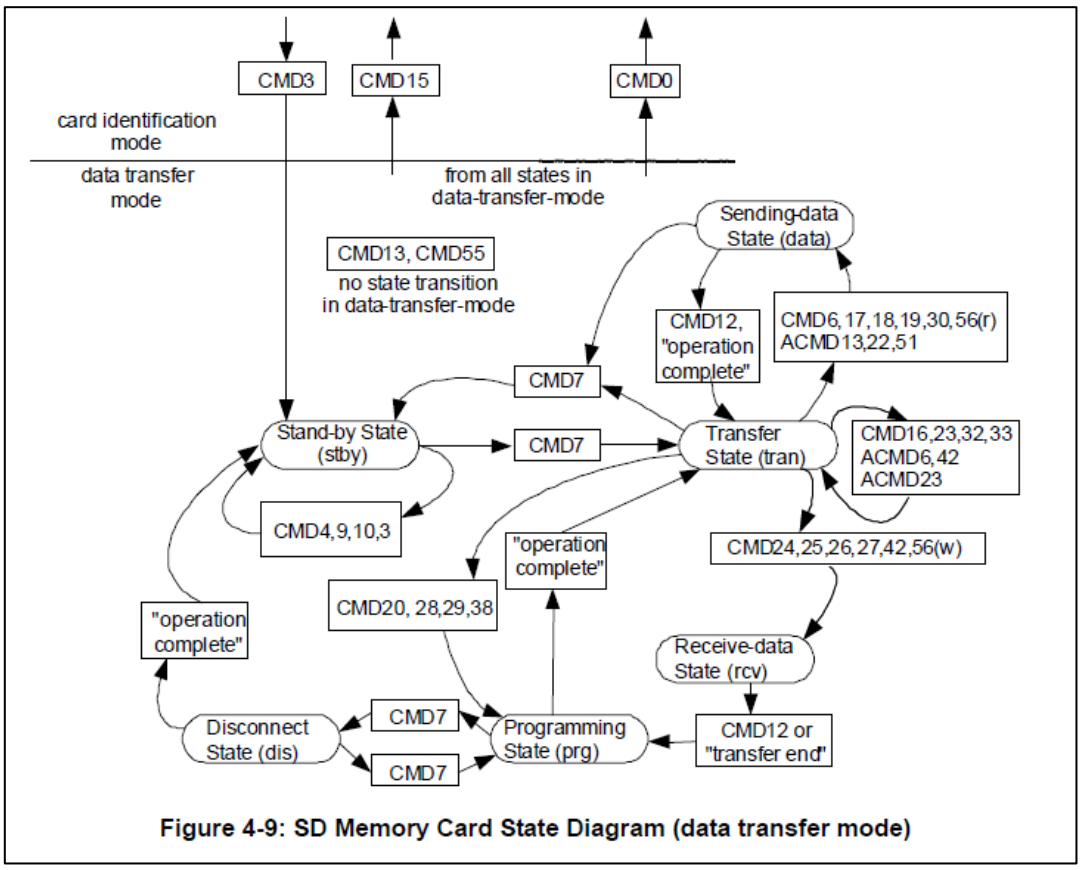


Figure 4-9: SD Memory Card State Diagram (data transfer mode)

Extracted from the SD Specifications Part 1 Physical Layer Simplified Specification Version 3.01.

7.1.2. Definitions for Response Data Bytes

Response Data	Description
Flash ID	NAND Flash Type
IC Version	Controller Version
FW Version	Firmware Version
CE Number	Number of chip enables active
Maximum Bad Block Replacement	Number of spare blocks remaining
Bad Block Count per CE	Number of initial & new bad blocks per chip enable
Good Block Rate (%)	Percent of total blocks that are still marked good
Total Erase Count	Total number of block erases at the card level
Calculated Remaining Card Life	[(Rated P/E cycles – Current Erase Count) / Rated P/E Cycles] * 100%
Average Erase Count	Average erase count over all blocks
Minimum Erase Count	Minimum erase count over all blocks
Maximum Erase Count	Maximum erase count over all blocks
Power Cycle Count	Number of normal power up sequences
Abnormal Power Down Count	Number of unexpected power interruptions
Total Refresh Count	Total read refresh count
Product “Marker”	Product type

7.2. Direct Host Access via DLL for Windows or Linux Operating Systems

Note: Card must be in Idle state before and while accessing card as per steps below.

API entry:

```
int Get_Smart_Data(char drive_letter, unsigned char *buffer, int buffer_len, int *bytes_read);
```

Arguments:

1: Drive letter is a character of the drive letter, i.e. ‘E’
2: buffer is a pointer to a pre-allocated array to store SMART data, min 512 bytes
3: buffer_len indicates to the API the size of the buffer, typically it is 512 bytes
4: bytes_read indicates the number of bytes returned in the buffer

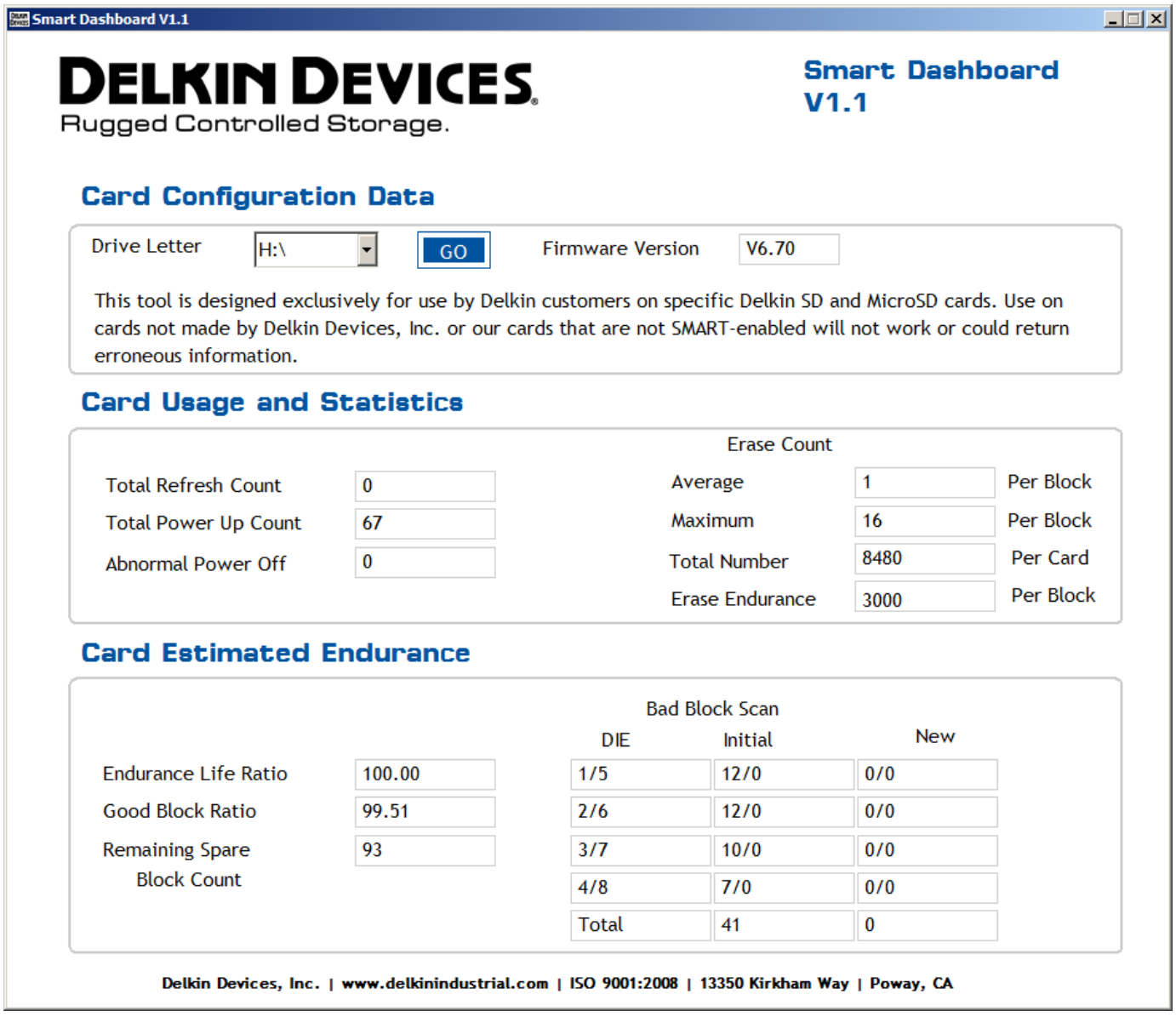
Return Value:

0 is success; Non zero is fail, with the following definitions:

1: "Initial Command Flow Fail"
2: "Read Capacity Fail"
3: "Switch To Vendor Mode Fail"
4: "Send Smart Info Command Fail"
5: "Get Command Response Fail"
6: "Command Response Info Incorrect"
7: "Read Command Info Fail"
8: "Check Command State Fail"
9: "Close Command Flow Fail"

7.3. Access via Delkin SMART Dashboard Utility

Delkin customers will be able to download the Delkin SMART dashboard utility (for Windows OS only) at www.delkinindustrial.com on the Engineering Specification page, or by contacting your Delkin Devices Account Manager. SMART data is accessed by inserting a card in a USB reader or directly in a laptop SD slot (with an SD adapter.) Below is a screen shot of the dashboard with sample data:



Instructions for use:

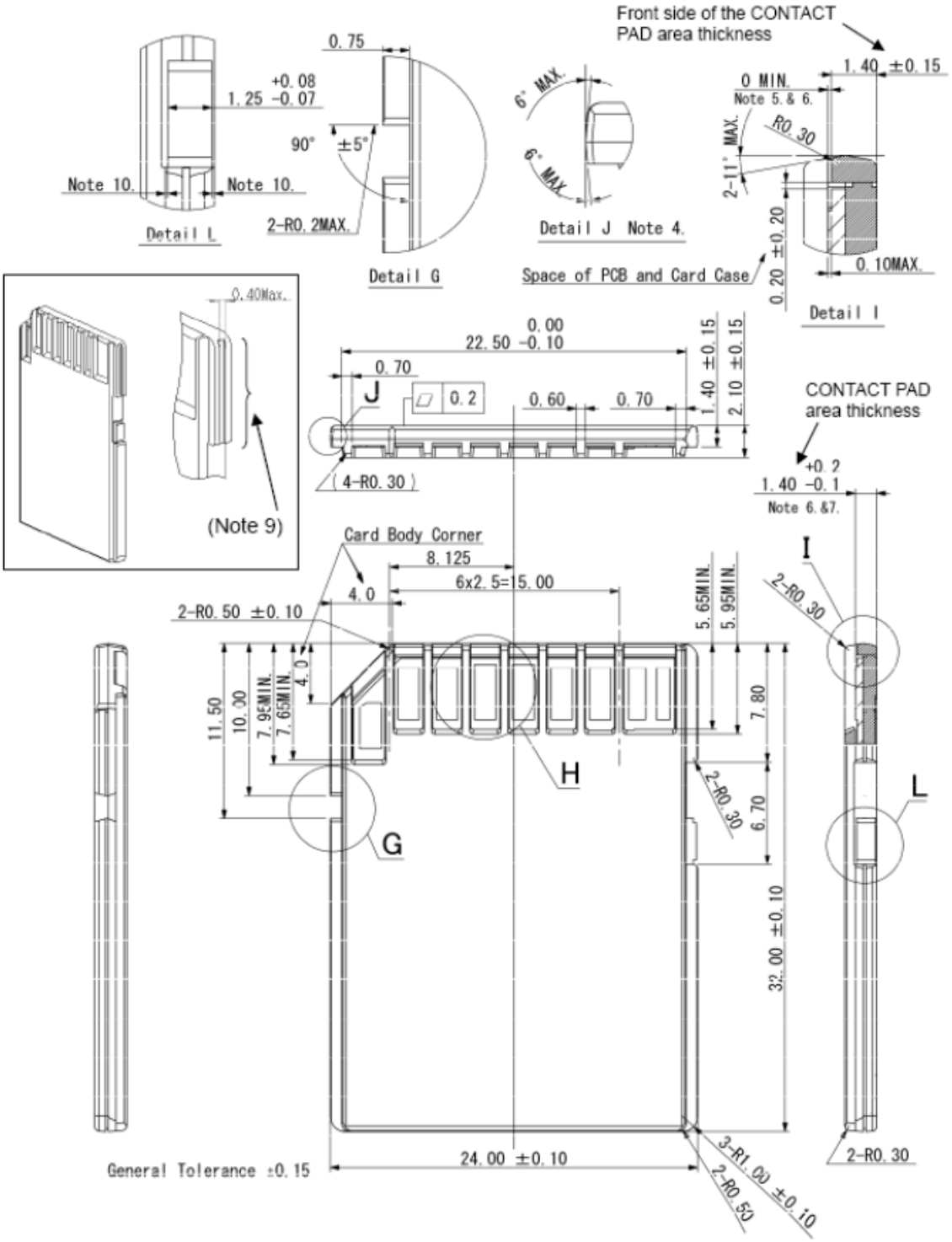
1. Insert microSD in card reader or in SD slot on laptop (in SD adapter)
2. Select appropriate drive letter on Dashboard
3. Click “Go”

7.3.1. Dashboard Field Descriptions

Response Data	Description
FW Version	Firmware Version
Total Refresh Count	Total read refresh count
Total Power Up Count	Number of normal power up sequences
Abnormal Power Off	Number of unexpected power interruptions
Average Erase Count	Average erase count over all blocks
Maximum Erase Count	Maximum erase count over all blocks
Total Erase Count	Total number of block erases at the card level
Erase Endurance	Flash program / erase cycle rating per block
Endurance Life Ratio	[(Rated P/E cycles – Current Erase Count) / Rated P/E Cycles] * 100%
Good Block Ratio	Percent of total blocks that are still marked good
Remaining Spare Block Count	Number of spare blocks remaining
Bad Block Scan - Initial (per die)	Bad blocks in flash from inception, prior to card use
Bad Block Scan - New (per die)	Bad blocks created after card use

8. PHYSICAL DIMENSIONS

Dimension: 32mm(L) x 24mm(W) x 2.1mm(H)



WARNING: This product may contain chemicals known to the State of California to cause cancer, birth defects, or other reproductive harm. For more information go to www.p65warnings.ca.gov.

